Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A cache system for a computer system, comprising:

a first cache for storing a first plurality of instructions;

a second cache for storing a second plurality of instructions;

wherein each instruction of the first plurality has an associated counter, and wherein when a first instruction of the first plurality is accessed, a first associated counter is incremented; and

wherein when the first associated counter reaches a threshold, the first instruction of the first plurality is copied into the second cache.

2. (Currently amended) The cache system of claim 1, wherein each instruction of the second plurality has an associated counter, and wherein when an instruction of the second plurality is accessed, all other counters of the second ~~first~~ plurality are decremented.

3. (Original) The cache system of claim 1, wherein the first instruction of the first plurality is accessed from the second cache.

4. (Canceled)

5. (Original) The cache system of claim 1, wherein the first cache is an instruction cache and the second cache is fully associative and follows a least recently used policy.

6. (Original) A method of managing cache in a computer system, comprising the steps of:

checking for a first instruction in a first cache, wherein each instruction in the first cache has an associated counter;

if the first instruction is found in the first cache, incrementing a first associated counter;

comparing a value of the first associated counter to a threshold;

if the first associated counter exceeds the threshold, moving the first instruction from the first cache to a second cache.

7. (Original) The method of claim 6, further comprising the step of:

accessing the first instruction from the second cache.

8. (Original) The method of claim 6, wherein each instruction of the second cache has an associated counter, and wherein when an instruction of the second cache is accessed, all other counters of the second cache are decremented.

9. (Canceled)

10. (Original) The method of claim 6, wherein the first cache is an instruction cache and the second cache is fully associative and follows a least recently used policy.

11. (Original) A computer program product in a computer readable medium, comprising:

first instructions for checking for a first line of data in a first cache, wherein each line of data in the first cache has an associated counter;

second instructions for, if the first line of data is found in the first cache, incrementing a first associated counter;

third instructions for comparing a value of the first associated counter to a threshold;

fourth instructions for, if the first associated counter exceeds the threshold, moving the first line of data from the first cache to a second cache.

12. (Currently amended) The computer program product of claim 11, further comprising the step of:

accessing the first line of data ~~instruction~~ from the second cache.

13. (Currently amended) The computer program product of claim 11, wherein each line of data ~~instruction~~ of the second cache has an associated counter, and wherein when a line of data ~~an instruction~~ of the second cache is accessed, all other counters of the second cache are decremented.

14. (Canceled)

15. (Original) The computer program product of claim 11, wherein the first cache is an instruction cache and the second cache is fully associative and follows a least recently used policy.

Amendments to the Drawings:

Figure 2 has been amended to delete FSP processor 214, FSP flash memory 220, FSP DRAM 221, NVRAM 222, and super I/O controller 223, their associated reference numbers, and connecting lines.

Attachment: Replacement Sheet
Annotated Sheet Showing Changes